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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,275	10/03/2005	Yasuyuki Matsui	4917/PCT	4014

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EXAMINER	
LUKE, DANIEL M	

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/552,275	MATSUI ET AL.	
	Examiner	Art Unit	
	Daniel Luke	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 03 October 2005 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/3/2005 & 11/13/2006.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 10/3/2005.

Currently, claims 1-8 are pending.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

IDS

The information disclosure statements (IDS) submitted on 10/3/2005 and 11/13/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Howard et al (US Patent 6,890,863).

Pertaining to claim 1, Howard shows, while referring to FIG. 4, a method of manufacturing single-crystal semiconductor blocks, wherein small-diameter single-crystal semiconductor blocks of a relatively small diameter (404) for slicing off single-crystal semiconductor wafers of a relatively small diameter desired by users are cut out from a large-diameter single crystal semiconductor block of a relatively large diameter (401).

Pertaining to claim 2, Howard shows the method of manufacturing single-crystal semiconductor blocks according to claim 1, wherein said semiconductor is a III-V group compound semiconductor (column 3, lines 10-14).

Pertaining to claim 6, Howard shows the method of manufacturing single-crystal semiconductor blocks according to claim 1, wherein a total cross-sectional area of a plurality of said small-diameter single-crystal semiconductor blocks cut out from said large-diameter single-crystal semiconductor block corresponds to at least 50% of a cross-sectional area of said large-diameter single-crystal semiconductor block (FIG. 4 clearly shows the total cross-sectional area of small-diameter blocks 404 is more than 50% of the cross-sectional area of the large-diameter block 401).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Howard et al (US Patent 6,890,863) in view of Sarayama et al. (US Patent 6,780,239).

Howard shows the method of claim 1.

Howard fails to show the large-diameter single crystal semiconductor block has a thickness of at least 10 mm.

However, Sarayama teaches in column 4, lines 24-30, that a GaN crystal is grown to a thickness of several tens of millimeters, followed by the subsequent slicing of the crystal to form wafers.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the large-diameter semiconductor block of Howard at a relatively large thickness of several tens of millimeters, as taught by Sarayama, with the motivation that a thicker crystal allows for more wafers to be sliced in comparison to a thinner crystal. Thus, fewer crystals would need to be grown in order to produce the same number of wafers.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Howard et al. (US Patent 6,890,863).

Howard shows the method of claim 1, but fails to show, in his invention, that the small-diameter semiconductor block is cut out of the large-diameter semiconductor block by means of

an electric discharge machining method, a wire saw method, a grinding method by means of a cylindrical core, or a band saw method.

However, Howard does teach in column 1, lines 16-18 that a wire saw is used to cut smaller semiconductors from large semicondctors.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a wire saw to cut the small-diameter semiconductor block from the large-diameter semiconductor block in the method of Howard, with the motivation that such a process is well-known in the art for such an application (column 1, lines 16-18).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Howard et al (US Patent 6,890,863) in view of Suda (US Patent 5,824,153) and Smith (US Patent 4,343,832).

Howard shows the method of claim 1, wherein at least four small-diameter single crystal semiconductor blocks are cut out from the large-diameter single-crystal semiconductor block (shown in FIG. 4).

Howards fails to show that the small-diameter single crystal semiconductor blocks have a diameter of at least 2 inches and the large-diameter single-crystal semiconductor block has a diameter of at least 5 inches.

However, Smith teaches in column 1, lines 33-35 that 2-inch diameter wafers can be used in semiconductor processes. Suda teaches in column 1, lines 28-29 that ingots are formed at a diameter of 8 inches.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the method of Howard to an 8-inch ingot, as taught by Suda, to ultimately form 2-inch wafers, as taught by Smith, for the reasons that 8-inch ingots are heavy, and are thus

difficult if not dangerous to handle (Suda column 1, lines 40), whereas a 2-inch ingot is easier to handle, and a wafer formed from a 2-inch ingot is less prone to breakage during processing (Smith column 1, lines 33-35).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Howard et al (US Patent 6,890,863) in view of Nakamura et al. (US Patent Application 2003/0041796).

Howard shows the method of claim 1.

Howard fails to show defective parts included in any cross-sectional area of said large-diameter single-crystal semiconductor block correspond to at most 65% of said cross-sectional area.

However, Nakamura teaches in [0102] that a 200 mm single-crystal silicon ingot can be produced to such that at least 55% of the entire wafer plane is defect-free.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the ingot in which 55% of the wafer plane is defect-free, as taught by Nakamura, as the large-diameter single-crystal semiconductor block of Howard, with the motivation that the elimination of defects leads to a decreased chance of performance deterioration in a semiconductor device (Nakamura [0003]).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Howard et al (US Patent 6,890,863) in view of van der Muehlen et al. (US Patent 6,489,626).

Howard teaches the method of claim 1.

Howard fails to teach that the small-diameter single-crystal semiconductor blocks are formed to have at lease any of an orientation flat, an index flat, and a notch for easy determination of its crystal orientation.

However, van der Muehlen teaches in column 1, lines 38-52 that a wafer flat or notch is typically formed in a wafer to determine its crystal orientation during a handling process.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form a wafer flat or notch in the small-diameter single-crystal semiconductor blocks of Howard, as taught by van der Muehlen, with the motivation that such flats are notches are useful in subsequent processes, such as controlling a channel formed by implanted ions (van der Muehlen column 1, lines 49-52).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Luke whose telephone number is (571) 270-1569. The examiner can normally be reached on Monday through Friday 7:30 a.m. to 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DL
9/13/2007

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